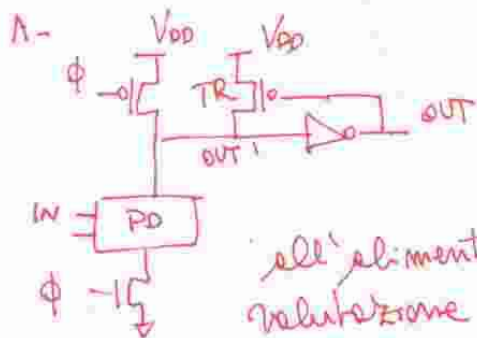
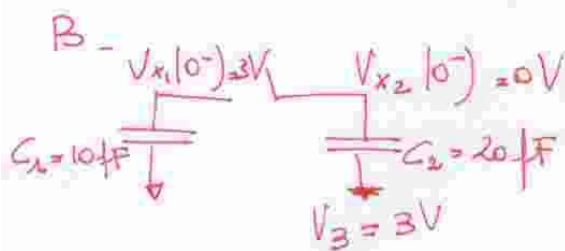


Circuiti Elettronici Digitali: L-A 13-07-05



Si tratta di un circuito statico. Tale proprietà è dovuta alla presenza del transistor TR che collega il nodo OUT all'alimentazione quando, in fase di valutazione tale nodo non è scaricato a massa.

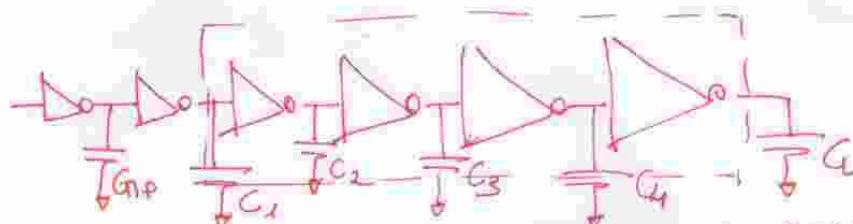


$$10 \text{ pF} \cdot 3 \text{ V} + (0 - 3) \text{ V} \cdot 20 \text{ pF} = 0$$

$$= V_x \cdot 10 \text{ pF} + (V_x - 3) \text{ V} \cdot 20 \text{ pF}$$

$$V_x = 1 \text{ V}$$

C-



$$\frac{C_L}{C_{np}} = \frac{1000 \text{ pF}}{10 \text{ pF}} = 100$$

$$G = \sqrt[5]{100} = 2,51 ; S_{np} = \frac{C_{np}}{C_{ox} \cdot L^2 \cdot 3} = 7,887$$

$$S_{M1} = 19,80 ; S_{P1} = 39,6 ; S_{M2} = 49,70 ; S_{P2} = 99,4 ;$$

$$S_{M3} = 124,74 ; S_{P3} = 249,48 ; S_{M4} = 313,10 ; S_{P4} = 626,2$$

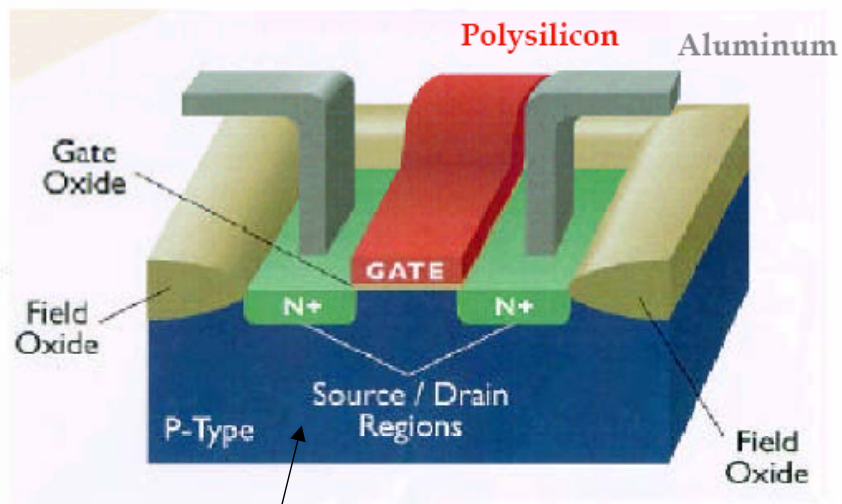
$$C_1 = 25,10 \text{ pF} ; C_2 = 63,01 \text{ pF} ; C_3 = 158,15 \text{ pF} ; C_4 = 397,01 \text{ pF}$$

$$\tau_{tot} = 4 \times G \times \tau_{np} = 13,06 \text{ nsec}$$

MOS transistor

polisilicio per il contatto di gate

Ossido di gate che costituisce l'isolante della capacità di gate

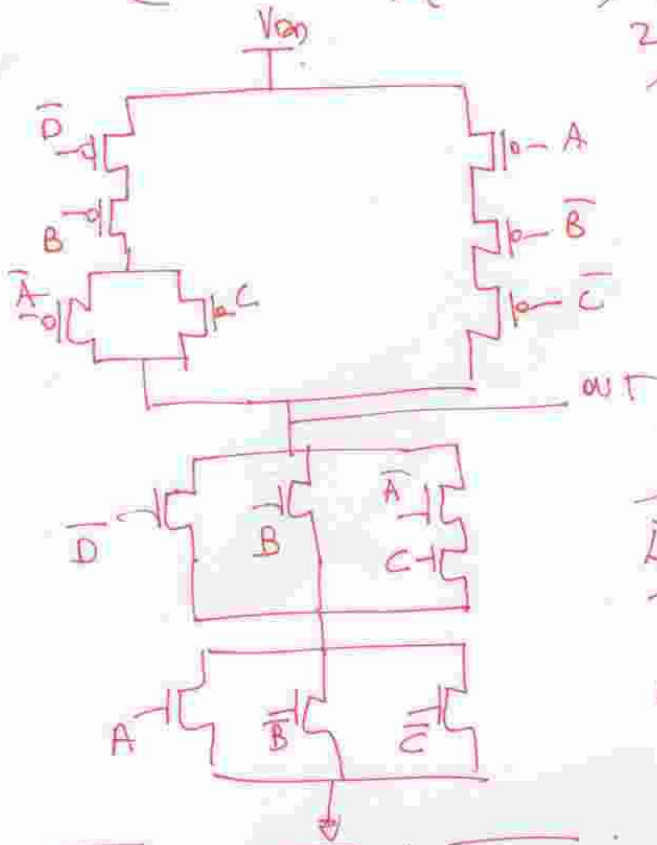


Silicio monocristallino drogato tipo p

ossido di campo per isolamento tra i

$$E // A = \overline{[D \cdot \overline{B} | A + \overline{C}]} + (\overline{A} \cdot B \cdot C) = (\overline{D} + B + A + \overline{C}) \cdot (A + \overline{B} + \overline{C})$$

$$= (\overline{D} + B + \overline{A} \cdot C) \cdot (A + \overline{B} + \overline{C})$$



$$2) \tau_{rc} = \frac{2 \cdot 100 \text{ fF}}{\beta_p \cdot S_{p,eq}} \cdot 0,6211 =$$

$$= \frac{4 \cdot 10^{-15} \cdot 3}{10^{-6} \cdot S_p} \cdot 0,6211 = \frac{7,4532}{S_p}$$

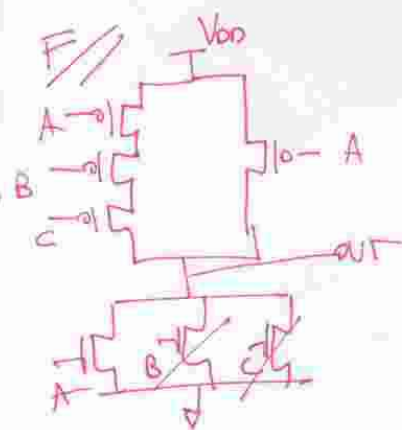
$$S_p \geq \frac{7,4532 \cdot 10^{-9}}{500 \cdot 10^{-12}} = 14,91$$

$$3) S_m \geq 7,455$$

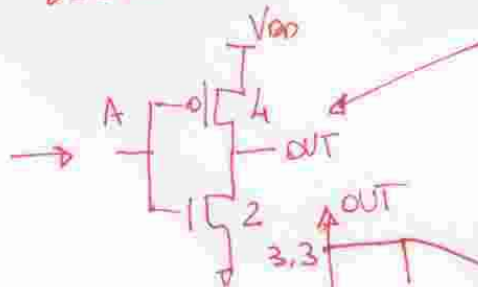
$$4) A = L^2 \cdot (7 \cdot 7,455 + 7 \cdot 14,91) =$$

$$= 19,178 \mu\text{m}^2$$

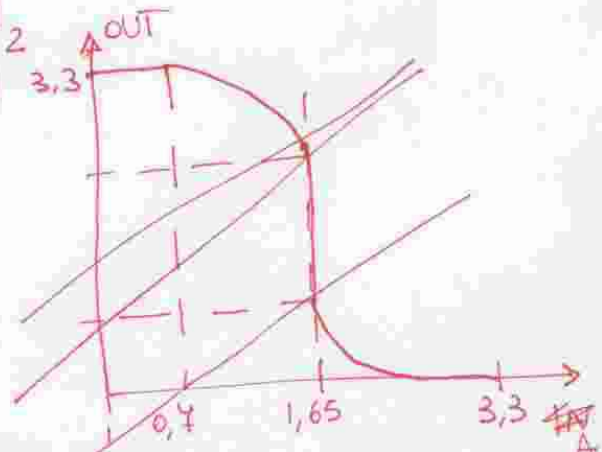
$$C_{in(A)} = C_{ox} \cdot L^2 \cdot 3(7,455) = 9,452$$



$$B=C=0 \quad S_p=3 \quad S_m=2$$



$$S_{p,eq} = \frac{S_p}{3} + S_m = \frac{4}{3} S_p = 4$$



2) $V_{IN} < 0,7V$ NMOS OFF, PMOS EQ LIN

$V_{IN} = 0,7V$ NMOS ON SAT, PMOS EQ LIN

$\left\{ \begin{array}{l} \text{NMOS SAT} \rightarrow \text{LIN} : V_{IN} - 0,7V = V_{OUT} \\ \text{PMOS LIN} \rightarrow \text{SAT} : V_{IN} - V_{DD} = V_{OUT} - V_{DD} \end{array} \right.$

$\rightarrow V_{IN} = 1,65V$

$$\left\{ \begin{array}{l} V_{OUT} = 1,65V + 0,7V = 2,35V \\ V_{OUT} = 1,65V - 0,7V = 0,95V \end{array} \right.$$

$N_{\text{LIN-SAT}}$ $N_{\text{SAT-LIN}}$

3) $V_{IN} = V_{OUT} = 1,65V$

A) $\beta_p' \cdot \frac{S_p}{3} = \beta_n' \cdot S_{nc}$ $\frac{S_p}{3} = 2 \cdot 2 \rightarrow S_p = 12$

$A_{2,PU} = L^2 \cdot 4 \cdot 3 = 12L^2$ $A_{2,PU} = L^2 \cdot 3 \cdot 12 = 36L^2$

In termini di area è meglio la soluzione che inserisce il transistor di dx comandato da A.