NETWORK-ON-CHIP ARCHITECTURES

XPIPES: Features

- Parameterizable network building blocks
  - Plug-and-play composable for arbitrary network topology
  - Design time tunable
- Pipelined links
- Source based routing
  - Street sign routing
  - Very high performance switch design
- Wormhole switching
  - Minimize buffering area while reducing latency
- Standard OCP interface

Written in synthesizable SystemC at the cycle accurate level
Irregular topology

SoC component specialization leads to the integration of heterogeneous cores

Ex. MPEG4 Decoder

- Non-uniform block sizes
- SDRAM: communication bottleneck
- Many neighboring cores do not communicate

- Risk of under-utilizing many tiles and links
- Risk of localized congestion

NI Architecture

Only one outstanding “Read”
Switch architecture

- Highly parameterized
- Buffering at the outputs with virtual channel support
- Deeply pipelined architecture
- Forward control flow (ACK/NACK protocol)
- Distributed error detection logic

- Aggregate bandwidth: 64 Gbit/s (32 bit links, 500 MHz)
- Estimated switch area (0.10 um) 0.33 mm²

Output port architecture

- Pipeline depth 7
- Parameterizable # of Virtual channels
- CRC-based error detection

I/O matching Arbitration Register arbiter Buffering Forward control Output arbiter
**Flow control**

- Transmission
- ACK and buffering
- NACK
- ACK/NACK propagation
- Memory deallocation
- Retransmission
- Go-back-N

**Network throughput and latency**
Aethereal

- Multiple tasks on the same processor
- Communication between tasks through FIFOs
- FIFO split between source and destination local memories

Guaranteed Throughput channel

Æthereal: features

- Conceptually, two disjoint networks
  - a network with throughput+latency guarantees (GT)
  - a network without those guarantees (best-effort, BE)
- Several types of commitment in the network
  - combine guaranteed worst-case behaviour with good average resource usage
**Router architecture**

- **Best-effort router**
  - Worm-hole routing
  - Input queueing
  - Source routing

- **Guaranteed throughput router**
  - Contention-free routing
    - synchronous, using slot tables
    - time-division multiplexed circuits
  - Store-and-forward routing
  - Headerless packets
    - information is present in slot table

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**Contention-free routing**

Use slots to
- avoid contention
- divide up bandwidth

The input routed to the output at this slot

input 2 for router 1 is output 1 for router 2
**Best-effort router**

- Virtual input queuing
- Avoid head-of-line blocking problem
- Link utilization increased from 59 to 100%

**Overall architecture**

Data is sent to the proper router
Best effort packets used to program slot table
GT packets are prioritized by an arbitration stage
**Router implementation**

- **Memories (for packet storage)**
  - Register-based FIFOs are expensive
  - RAM-based FIFOs are as expensive
    - 80% of router is memory
  - Special hardware FIFOs are very useful
    - 20% of router is memory

- **Speed of memories**
  - registers are fast enough
  - RAMs may be too slow
  - Hardware FIFOs are fast enough

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**Layout**

- Data packets
- Flow control
- Programming packets
Results

- 5 input and 5 output ports (arity 5)
- 0.25 mm2 CMOS12
- 500 MHz data path, 166 MHz control path
- flit size of 3 words of 32 bits
- 500x32 = 16 Gb/s throughput per link, in each direction
- 256 slots & 5x1 flit fifos for guaranteed-throughput traffic
- 6x8 flit fifos for best-effort traffic

Low Power Design

Energy Efficient Network-on-Chip Design
**On-chip communication**

- Interconnects are (and will be even more) large contributors to on-chip energy
- Interconnect-oriented design methodology at all layers of IC design (system to physical)
- Signal integrity issues. Need for energy-efficient and reliable communication
  - error tolerance instead of error avoidance
  - error recovery techniques at higher layers

*Networks-on-Chip exhibit potentials for low power on-chip communication*

**Interconnect-oriented design methodologies**

- **NETWORK LEVEL**
  - Data routing, Multiple access
  - Error Detection and Correction

- **SYSTEM LEVEL**
  - Adaptive supply voltage links
  - Communication based DPM

**ENERGY EFFICIENT AND RELIABLE SoC COMMUNICATION ARCHITECTURE**

- **ARCHITECTURE LEVEL**
  - Bus isolation, Topology selection
  - Interface Design and Synthesis

- **CIRCUIT LEVEL**
  - Low swing signaling, buffer sizing
  - Current mode signaling
Circuit level techniques

- Two-inverter configuration with rail-to-rail signal swing
- \( E(\text{clock}_\text{cycle}) \propto C V_{dd} V_{sw} \)
- Full swing: scaling \( V_{dd} \) reduces energy quadratically
- Low swing signaling
  - reduced energy
  - reduced propagation time
  - reduced noise margins
  - increased complexity and delay

Low swing signaling

- Conventional level converter
- Need for an additional reference voltage
- receiver behaves as a differential amplifier
- very robust wrt noise
- becomes slow for very low swings
Differential interconnect

- Differential signaling. Allows to further reduce swing
- Wire overhead
- Additional clock signal
- Receiver charged and discharged at each clock cycle
- LVDS (Low Voltage Differential Signaling) standard interface for low swing (330 mV) and high performance (from 100 Mbps to > 1 Gbps) signaling (mainly I/O signaling)

Pseudo-differential interconnect

- Single wire routing
- Retains most advantages of DIFF interconnects
  - Low input offset, good sensitivity
- Not sensitive to Vdd supply noise
- Degradation sources:
  - Mismatch between input TNs pairs
  - Differences in driver/receiver REFs
Current-mode signaling

- Digital levels represented as direction and/or magnitude of current
- Low voltage swing on the interconnect – good for capacitive lines

Current vs voltage sensing

- The speed of the current mode receiver will be faster than the voltage mode for long interconnect because:
  - The signal sees a low-impedance current-sensitive load.
  - This eliminates the cumbersome charging and discharging of the capacitance.
  - Current-mode signaling is more energy and performance-efficient
Current vs Voltage sensing

- Low impedance termination

- The interconnect is driven using low-swing technique at the driver
- The voltage swing on the line is minimized because of the low-impedance current sensing termination.

Example

- Driver has inverted transistors, thus reducing swing to Vdd – 2Vth
- Current receiver formed by current comparator and Current-Controlled Voltage Source (CCVS) Amplifier
Current mode signalling

- **Advantages**
  - Power supply noise reduced
    - Low swing signaling reduces the current spikes at the driver end for the current sensing technique.
    - Current sense receiver draws static current which significantly reduces the current spikes from the supply.
    - If receiver is a differential amplifier, power supply noise is made common mode
  - Very low voltage swings (as low as 100 mV) and reliable operation
  - Very low power consumption
  - Very high bandwidth

- **Disadvantages**
  - High static power consumption – bad for low data activity
  - Analog design

Communication Architecture

*Shared buses are energy/power inefficient:*
- Entire load capacitance switched at each clock cycle
- High frequency bus operation to get high throughput

*Workarounds.............................*

- Bus splitting

Dual ported splitters retain overall bus functionality
**AMBA BUS**

- **AMBA AHB**
  - High performance
  - Pipelined operation
  - Multiple bus masters
  - Burst transfers
  - Split transactions

- **AMBA ASB**
  - High performance
  - Pipelined operation
  - Multiple bus masters

- **AMBA APB**
  - Low power
  - Latched address and control
  - Simple interface
  - Suitable for many peripherals

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**IBM CoreConnect**

- **Device Control Register Bus (DCR)**
  - 32-bit bus for initiating peripherals
  - Saves PLB and OPB bandwidth

- **Processor Local Bus (PLB)**
  - 32-bit address, 64-bit data
  - Primary high-bandwidth bus interfacing “directly” with the processor

- **On-chip Peripheral Bus (OPB)**
  - 32-bit address, 32-bit data
  - Lower bandwidth bus interfacing to system peripherals
**Processor Local Bus (PLB)**

- High performance, synchronous on chip bus
- Deep pipelined read and write operations
- Max utilization of 2 data transfers per cycle
- 4 priority levels bus access requests
- Up to 16 master devices
- Daisy-chained DCR bus for configuration and system status check

**Bus splitting**

- AMBA bus and CoreConnect use bus splitting
- Energy savings from 16 to 50%
  - total load capacitance split
- Concurrency increase

**CRITICAL DESIGN ISSUES**

- Where and how often to split a bus?
- Floorplanning issues
**Router-based architecture**

- Used at the board-level to interconnect blocks in a MM node
- Fully or partially connected crossbar

**ADVANTAGES:**
- Reduced capacitive loading due to block isolation
- Increased communication parallelism
- Design time flexibility
- Energy scalability

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**Networks-on-Chip**

**Potentials for**
- structuring top level wires
  - better noise control
  - Less coupling power
- Power efficiency can be achieved by instantiating application specific NoCs
**Example: MPEG4 decoder**

- Core graph representation with annotated average communication requirements

**NoC Floorplans**

- General purpose: mesh
- Application specific: centralized
- Application specific: distributed
**Performance, area and power**

Less latency and better Scalability of custom NoCs

- Relative link utilization
  - (customNoC/meshNoC): 1.5, 1.55
- Relative area
  - (meshNoC/customNoC): 1.52, 1.85
- Relative power
  - (meshNoC/customNoC): 1.03, 1.22

**System level techniques**

*Communication based power management*

1. Static system configuration
2. Communication architecture monitors system status
3. Communication architecture drives IP core status
   *(run-time frequency and voltage scheduling)* for energy efficient computation
Adaptive Low-power transmission scheme

Dynamic voltage scaling applied to on-chip interconnects