Practical Testing of Integrated Circuits

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Outline of the talk

1. Introduction
2. Test Hardware
3. Test Flow
4. Practical Problems
5. It does not work, now what?
6. Challenges
7. Final Words
Motivation

Testing is how you make money in the IC business

Customers want working chips

- We are in the business of selling integrated circuits.
- We must make sure that (nearly) all chips we sell, work.
- The customers are not very patient.
Even more Motivation

You need to test each and every chip you manufacture

**Production will not have 100% yield**

- It’s a cost issue.
- It is **cheaper to test all** chips, than making sure that there are no manufacturing errors.
- Contrary to *other* production flows, material costs are irrelevant.
- We will **not** try to **repair** not-working chips.
Economy of Finding Defects

The earlier we find the error, the less we pay

Depending on where we find the error, it will cost us differently:

- \(0.01\) \$ when detected early in production
- \(0.1\) \$ when detected on die
- \(1\) \$ when detected after packaging
- \(10\) \$ when detected on the board
- \(100\) \$ when detected in the system
- \(1000\) \$ when detected by the customer
Challenges for Testing

Testing is becoming more difficult

- Newer chips contain more parts, requires more effort to test
Challenges for Testing

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- Newer chips contain more parts, requires more effort to test
- Testing is time consuming.
  - Chip has to come to tester (mechanically)
  - Chip will be tested
  - Chip will be either labelled good (sold) or bad (thrown away).

If one operation takes about 8 seconds, we can only test 10,000 chips a day.
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- Faster chips require more precise measurements, more difficult, more expensive.
Different Test Types

The goals and requirements are different

- **Production Tests**
  Used for determining which chip works and which does not work.

  - **Speed**

Production Tests

Production Tests are used for determining which chip works and which does not work. They focus on speed, measuring the limits of the chip, and setting up the production test programs.
Different Test Types

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- **Production Tests**
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- **Prototyping**
  Used to measure the limits of the chip, and to set up the production test programs
  - **Observability**
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- **Debugging**
  Used to find why a particular chip is not working.
  - **Observability**
  - **Controllability**
Chips on a Wafer, Our Raw Product
Different Test Stages I

Process Control Monitors

- Placed on the wafer between actual chips
- May have patterns for optical testing
- Usually includes diodes, transistors, ring oscillators for parameter extraction
Different Test Stages II

On Wafer Test

- Prober cards make contact with the wafer
- Basic short tests are made to test quality of the chip
- Modern chips use laser trimming at this stage to calibrate critical (clock) delays.
Packaged Test

- In any case chips will be tested in the package.
- Loader robots bring the chips to the tester.
- The chip is tested comprehensively.
- This may be done away from the manufacturing site.
Stress Tests

- **Humidity**
  Increased Humidity may effect the packaging. Storing chips at hot/humid places may result in failures.
Different Test Stages IV

Stress Tests

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- **Temperature**
  Chips work slower at high temperatures. Temperature tests ensure correct operation at all operating temperatures.
Different Test Stages IV

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- **Burn In**
  Most failures occur within the first few months of operation. Burn in tests are used to sort out these failures.
Different Test Stages IV

**Stress Tests**

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- **Burn In**
  Most failures occur within the first few months of operation. Burn in tests are used to sort out these failures.

- **Aging**
  Proper operation needs to be guaranteed for 10 to 30 years. Accelerated aging tests are made to see if the chips would work for this time period.
Test Hardware

Basic Idea

- Apply stimulus vectors
- Sample the outputs
- Compare outputs to expected responses
- **Chip works if results match**
### Simple Idea

- Memory to store stimuli
- A driver to apply stimuli
- A receiver to observe the output
- Memory to store expected responses
- Comparator to detect differences
Architecture

- Each pin can be programmed to be input/output
- Adjustable logic threshold
- High precision timing
Test Hardware

Very Large Equipment

- **Multiple channels:**
  128 - 1024

- **High speed:**
  200 MHz - 1 GHz

- **Many vectors:**
  1 Mvectors - 256 Mvectors

- **High precision:**
  50-200 ps time accuracy
Connectivity Test

Can we access the chip

- Tests the ESD structures
- Do we have physical access to the chip?
- Test board is ok, bonding wires are ok.
Current Consumption

\[ P_{total} = P_{dynamic} + P_{static} \]
\[ P_{dynamic} \sim \alpha \cdot C \cdot f \cdot V_{dd}^2 \]

Parameters

- \( \alpha \): Stimulus vectors
- \( C \): Netlist
- \( f \): Frequency
- \( V_{dd}^2 \): Operating Conditions
Current Tests

Testing Current Consumption

- Need to find correct vectors
- Activity $\alpha$ directly determines the consumption.
  - A processor executing NOPs will not consume much power.
- Increased power consumption may show potential problems before other tests
- **IDDQ tests**
  increased static power consumption may reveal shorts.
Stuck at Faults

Single Stuck at Fault Model

It is assumed that there is a single fault in the circuit that is either:

- **Stuck-at-0**
  The gate input/output will always remain at logic-0

- **Stuck-at-1**
  The gate input/output will always remain at logic-1

Test vectors are created to verify if there is a stuck-at fault in the circuit.

*This is just a model, it is not necessarily physical*
Scan Tests

Main idea
Find input vectors that will have different outputs if one gate is not working correctly
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Find input vectors that will have **different** outputs if one gate is not working correctly
Scan Chains

Sequential elements

Scan chains convert the sequential elements to programmable inputs and observable outputs.
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Performing Scan Tests

1. A circuit with scanable flip-flops is used
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4. The scan vector is clocked in serially
Scan Test Flow

Performing Scan Tests

1. A circuit with scanable flip-flops is used
2. Scan vectors are generated by special programs
3. Normal operation is stopped and circuit is brought into scan mode
4. The scan vector is clocked in serially
5. The circuit is run in normal mode for 1 cycle
Scan Test Flow

Performing Scan Tests

1. A circuit with scanable flip-flops is used
2. Scan vectors are generated by special programs
3. Normal operation is stopped and circuit is brought into scan mode
4. The scan vector is clocked in serially
5. The circuit is run in normal mode for 1 cycle
6. Once again scan mode, and the response is clocked out serially
7. Process repeated for all vectors
## Parameters of Scan Test

- **Fault Coverage**
  Percentage of potential faults that can be detected

- **Number of faults**
  Total number of potential fault locations in the circuit (depending on the model).

- **Number of scan vectors**
  Number of vectors needed to achieve the given fault coverage

- **Longest scan path**
  Number of flip-flops connected in the longest scan chain.

- **Number of clock cycles**
  Number of clock cycles required to perform the scan test.
About Scan Test

Scan Test:

- **does not check functionality**
- verifies that each gate is manufactured correctly
- success depends on the fault coverage.
- not all possible faults can be detected
- does not reveal timing information.
Some Example Numbers

Assume that we want to sell 500,000 chips, that has 2 million gates and was manufactured with a yield of 85%.

- We need to manufacture 588,250 chips, **88,250 will not work**.
- There will be roughly 4,000,000 fault locations
- Assume a 99% fault coverage: **40,000 faults will not be detected**.
- Roughly **900 defective units will be sold**
**Does the circuit work?**

- Based on applying stimuli and comparing the outputs.
- Has generally poor coverage.
- Vector generation is very important.
- However, is the basis of most other tests (for example maximum clock frequency):
  - A functional test is run.
  - Frequency is increased.
  - The test is re-run.
  - The last *working* frequency is the maximum clock frequency.
**ATI timing**

![ATI Timing Diagram]

**Timing model**

- **A** Stimulus application time
- **T** Response acquisition time
- **I** Active clock edge

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**ATI**

- **Period**
- **Stimulus Application**
- **Response Acquisition**
- **Active Clock Edge**
Input to Output

- Is tricky, input and output pads have large delays
- Is measured by reducing the time difference between stimulus application and response acquisition.
- If possible should be avoided in fast circuits

Measuring Timing

[Diagram showing input to output timing with labels for \( t_{pd,in\to out} \), \( t_{input} \), and \( t_{output} \).]
Measuring Timing II

Input to Register

- **Setup time**
  The time the signal has to be stable at the input before the active clock edge

- **Hold time**
  The time the signal has to remain at the input after the active clock edge

- Measured by moving the stimulus application time.
Register to Output

- **Output Propagation Delay**
  The longest time it takes for the output to settle after an active clock edge

- **Contamination Delay**
  The shortest time it takes for the output to change after the active clock edge

- Measured by moving the response acquisition time.
Register to Register

- Is tricky, all other timings must be determined prior to this measurement.
- Is measured by reducing the clock period.
- Ideally, this should be the limiting timing constraint.
Voltage Levels

Tester has programmable:
- input low level
- input high level
- output threshold
  Everything below is zero
  Everything above is one
Input and Output Logic Levels

Parameters

\[ V_{IL} \] Input Low Level
\[ V_{IH} \] Input High Level
\[ V_{OL} \] Output Low Level
\[ V_{OH} \] Output High Level

\[ V_{OH} \] Output logic-1
\[ V_{OL} \] Output logic-0
\[ V_{IH} \] Input logic-1
\[ V_{IL} \] Input logic-0
Parametric (Shmoo) Plots
The 'Binning' Problem
Many problems

- Many test channels, large volume
  long connections to pins (20cm - 1m).
- Long cables have large capacitive loads
- Chip is not normally designed to drive these large loads
  increased I/O current, slower I/O
- Impedance mismatches
  reflections on the cable
Light speed is not so fast

300,000 km/s = 30 cm/ns (in vacuum)

Cable is crowded
- Many signals travel on the cable at the same time.
- Bi-directional signal acquisition is complicated.
Tester Memory

The memory is not unlimited

- Tester needs to store data for each clock cycle
- Memory is not so cheap
  (millions of dollars for test equipment)
- Fast memory is limited
  - The chip is idled until the memory is refreshed
  - break vectors are used for idling
- Break vectors are not always trivial
  (PLLs, local clock generators etc.)
It does not work, now what?

*It is important to find out why it does not work, wild, unprovable theories will not help*

**Debugging is part of the business**

- In production we simply throw away the bad chips.
- During prototyping we want to find out **why**, and correct as fast as possible.
Correcting the Metal Masks

**Metal Spins**

- Several 'spare' gates are placed 'unconnected' on the chip.
- If there are problems, these gates can be used to fix the problem.
- Only the metal mask needs to be reprogrammed. The **costly** lower layers can be kept the same. This is much cheaper than making a complete new chip.
- Most production chips, have several metal spins.
Complex designs offer a range of programmability options, that can be changed after production.

Most instruction decoders can be programmed

RAMs have several ’reserve’ cells. After testing defective cells can be replaced by the reserve cells by reprogramming the address decoders.

Reprogramming can be made by:
- Blowing fuses
- EEPROM structures
- Laser programming
Laser Cutting

Simple corrections

- Can evaporate material (only what is visible)
- Used to cut shorts
- Blow fuses
- Engrave serial numbers
- Trim resistances
Example: Rijndael Chip at ETHZ
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Focussed Ion Beam

Magic tool

- FIB is similar to a scanning electron microscope
- Gallium Ions are accelerated to the surface
- The reflecting ions/electrons can be used for imaging.
- The intensity can be increased to drill holes
- Gas concentration can be adjusted to deposit materials (Platinum, Oxide).
Challenges for Testing

Main Problems

- **Number of I/Os increase**
  
  \( \text{price}++ \)
Challenges for Testing

Main Problems

- **Number of I/Os increase**
  - (*price++*)

- **Number of devices on chip increase**
  - (*vectors++*, *time++*)
Challenges for Testing

**Main Problems**

- **Number of I/Os increase**
  \(\text{price}++\)

- **Number of devices on chip increase**
  \(\text{vectors}++\), \(\text{time}++\)

- **Devices get faster**
  \(\text{I/O complexity}++\), \(\text{time}–\)
Challenges for Testing

Main Problems

- Number of I/Os increase
  \((\text{price}++)\)

- Number of devices on chip increase
  \((\text{vectors}++ , \text{time}++)\)

- Devices get faster
  \((\text{I/O complexity}++ , \text{time}–)\)

Other Problems

- Variability
- Soft Errors
Solutions

Addressing Testing Problems

- **Redundancy**
  Add multiple copies for critical components, check all.

- **Error Detection and Correction**
  Check all operations for correctness, use coding techniques to correct errors.

- **Built-in Self-Test**
  Reduce testing complexity, by adding hardware to do a self test. This will reduce the external testing effort.
Final Words

Testing

- Testing is all about money.
- If you can not test a chip, you can not sell it.
- Many chips require more time for testing than it was required to design them.
- Design for Testability, is a general term that includes test considerations early into the design flow.
- Most of a modern industrial design flow is verification and test.