

Designers are faced by new challenges due to the complexity of future Multi-Processor Systems-on-Chip (MPSoCs). The design space is very large and many design alternatives need to be explored during architecture definition and tuning. Moreover, gigascale MPSoCs will be increasingly communication-dominated, therefore many efforts are being devoted to the development of aggressively scalable on-chip communication architectures. The research activity in our NoC group addresses both issues. On one hand, we are developing a flexible, functionally-accurate simulation environment for on-chip multi-processors (called MPARM), targeting high accuracy modelling and simulation of such devices. On the other hand, we are developing advanced on-chip interconnects leveraging network technology (generally known as “Networks-on-Chip”). Customized, domain-specific MPSoCs are our primary target and the Xpipes NoC has been designed in our group for this purpose.

Overall, we are building an infrastructure allowing us to compare in-house built as well as industrial advanced on-chip interconnects from a performance and power viewpoint, and to accurately analyze the MPSoC design space.

## **NETWORK-ON-CHIP ARCHITECTURES**

### **MOTIVATION**

As technology scales toward deep sub-micron, an increasing number of computational units will be integrated onto the same silicon die, posing tight communication requirements on the communication architecture. State-of-the-art on-chip interconnects are shared busses with central arbiters for serializing bus access requests. This simple solution has serious scalability properties, leading to critical performance penalties and energy inefficiencies as the number of integrated cores increases. There is a world-wide ongoing effort to design more scalable communication architectures, for instance leveraging network technology and adapting it to the on-chip scenario. The resulting architectures are known as “Networks-on-Chip” (NoCs) and have some promising features for application to gigascale systems-on-chip such as high modularity, scalability, potentials for energy savings (e.g., application-specific NoCs) despite the increased design complexity.

### **RESEARCH ACTIVITY**

We analyzed NoC design issues at different layers of abstraction. The first step was to address low level challenges in designing on-chip interconnects in presence of deep sub-micron technologies. Due to the increased role of noise sources such as crosstalk, power-supply noise, soft errors, etc., physical link design will not suffice to provide communication reliability, and the proper course of error-control actions will have to be taken at higher levels of abstraction. We focused on the data link layer, and investigated how communication reliability can be traded-off with energy, aware that the implementation of error correcting or detecting codes comes at a cost, both in terms of encoding and decoding logic and of additional link lines and transitions. We showed that error detecting schemes combined with retry procedures (e.g. retransmission of corrupted data) are more energy efficient than error correcting ones, due to the much higher decoding cost of this latter solution [1].

As a second step, we addressed system level NoC design and came up with a NoC architecture (called Xpipes) which can be used to instantiate application-specific MPSoCs [2]. Xpipes consists of parameterizable network building blocks that can be arbitrarily tuned and composed at instantiation time. This solution provides flexibility at the cost of an increased design complexity. Two relevant features of Xpipes are the use of deeply pipelined switches and of link pipelining, that decouples link throughput from the worst case link delay in the design. Therefore, operating frequencies in the multi-GHz range can be achieved. Xpipes is one of the most advanced NoC designs targeting heterogeneous MPSoCs with customized domain-specific communication

architectures. Its development is a joint effort of University of Bologna and Stanford University, and the final objective is to come up with a complete Xpipes-based NoC synthesis flow.

## **PUBLICATIONS**

[1] “Energy-reliability trade-off for NoCs”: D.Bertozzi, G.De Micheli, L.Benini, in “Networks on Chip”, edited by A. Jantsch, H. Tenhunen, Kluwer KAP, March 2003.

[2] “Xpipes: a latency insensitive parameterized network-on-chip architecture for multi-processor SoCs”, M.Dall’Osso, G.Biccari, L.Giovannini, D.Bertozzi, L.Benini, Int. Conf. On Computer Design, pp.536-539, October 2003.

## **ACADEMIC AND INDUSTRIAL COOPERATIONS**

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# **FUNCTIONALLY-ACCURATE MODELLING AND SIMULATION OF MULTI-PROCESSOR SoCs**

## **MOTIVATION**

Designers are faced by new challenges due to the complexity of future Multi-Processor Systems-on-Chip (MPSoCs). The increasing feature set of user applications, compounded with stringent requirements in terms of power consumption and scalability issues in the design of interconnects, determine the need for optimal choices in the deployment of embedded products. Such issues represent key factors to be investigated during architecture definition and tuning.

A flexible simulation environment, capable of accurately analyzing the interaction among cores and peripherals in a MPSoC, is an enabling factor for the design of the next generation of embedded devices.

## **RESEARCH ACTIVITY**

We developed MPARM, a multi-processor simulation platform, to explore design alternatives in the context of MPSoCs. The platform is both cycle-accurate and signal-accurate, allowing for detailed analysis of system performance based upon functional traffic.

MPARM is built around the ability of plugging different devices to a flexible environment. A variety of system IPs, interconnects, memories and peripheric devices can be easily mixed to explore performance tradeoffs. Processing cores include ARM, StrongARM and PowerPC ([1]), while interconnects span over a set of AMBA busses, STBus, and prototypes of future Networks-on-Chip (NoCs). Every system component can be thoroughly configured, e.g. processor cache type and size, memory latency, interconnect arbitration policy. Such flexibility enables interesting performance comparisons ([2]).

Thanks to support for scratchpad memories (SPMs) and DMA engines in addition to caches, MPARM adds further degrees of freedom to the design of memory hierarchies. System developers can optimally fit benchmark applications to available memory layers, resulting in better power/performance efficiency.

Support for energy models is provided, allowing, in combination with dynamic frequency/voltage scaling devices and energy-aware OS kernels, further research in the minimization of energy consumption.

## **PUBLICATIONS**

[1] L. Benini, D. Bertozzi, D. Bruni, N. Drago, F. Fummi, M. Poncino, "SystemC Cosimulation and Emulation of Multiprocessor SoC Designs", IEEE Computer, Volume: 36 Issue: 4, April 2003  
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[2] F. Poletti, D. Bertozzi, A. Bogliolo, L. Benini, "Performance Analysis of Arbitration Policies for SoC Communication Architectures", Journal of Design Automation for Embedded Systems, pp. 189-210, Vol. 8, June/Sep 2003

## **ACADEMIC AND INDUSTRIAL COOPERATIONS**

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